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## Automatic application-specific instruction-set extensions under microarchitectural constraints

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### ↑ ABSTRACT






Many commercial processors now offer the possibility of extending their instruction set for a specific application---that is, to introduce customised functional units. There is a need to develop algorithms that decide automatically, from high-level application code, which operations are to be carried out in the customised extensions. A few algorithms exist but are severely limited in the type of operation clusters they can choose and hence reduce significantly the effectiveness of specialisation. In this paper we introduce a more general algorithm which selects maximal-speedup convex subgraphs of the application dataflow graph under fundamental microarchitectural constraints, and which improves significantly on the state of the art.

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## ⤴ INDEX TERMS

### Primary Classification:

C. Computer Systems Organization

↳ C.1 PROCESSOR ARCHITECTURES

↳ C.1.3 Other Architecture Styles

### General Terms:

Algorithms, Design, Performance

### Keywords:

ASIPs, codesign, customisable processors, instruction-set extensions

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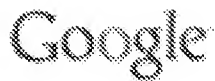


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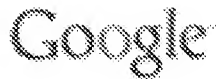
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